IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Vora

Art Unit: 2811

Examiner: S. Crane

Serial No. 08/654,760

Filed: May 29, 1996

For: VERTICALLY INTEGRATED FLASH EEPROM FOR GREATER DENSITY AND LOWER COST

Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Morgan Hill, California
November 29, 2002

DECLARATION OF ASHOK KAPOOR UNDER 37 CFR 1.132

Dear Sir:

Being hereby warned that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon, I hereby voluntarily make the following statements. The following statements made of my own knowledge are true, and all statements made on information and belief are believed to be true.

My name is Ashok Kapoor. I am not an inventor on the above identified patent application. My education is as follows. I obtained a masters degree and a PHD from the University of Cincinnati in 1981. My dissertation was in the area of solid state electronics and device physics for integrated transistor structures. My undergraduate studies were done at the India Institute of Technology where I graduated with a Bachelor of Science degree in electrical engineering in 1973.

My first job was at Fairchild Camera and Instrument's - Palo Alto Research Lab. I worked there from 1981 to 1988. My specialty was bipolar device design, integrated circuit processing and design of transistor device structures. After Fairchild was purchased by National Semiconductor, I worked for National untill 1988. From 1989 to 1991, I worked with Hewlett Packard. Since 1991, I have worked at various companies, always specializing in semiconductor device design, semiconductor device processing, process development, semiconductor device modeling and device physics. Since 1989, all my work has been on bipolar-CMOS or MOS devices. I also have work experience relating to nonvolatile memory device structure design and process design.

I have several patents in the flash EEPROM area (at least 3). Altogether I have 83 patents.

With respect to the Yoshida et al. patent, U.S. 5,049,956, Figures 3 and 5 are pertinent. The vertical structures shown in these figures cannot be built because a floating gate that thin cannot be made to stick up above the surface of the substrate as shown because of the processing difficulties I will discuss herein.

There are several major problems with Yoshida et al. patent approach in Figures 3 and 5 that make these structures impossible to build. First, it should be understood why the Yoshida et al. approach chooses to have the floating gate sticking above the top surface of the substrate. This design is intended to increase the ratio of the area of the capacitor between the floating gate and the control gate.These capacitors are shown as Capacitors C1 and C2, respectively, in Yoshida's Figure 1.It is evident from the figure that the capacitor C2 has greater area than the area of the capacitor between the floating gate and the channel region (C1 in Figure 1). Having capacitor C2 bigger than capacitor C1 is desirable because it increases the voltage drop across

the capacitor C1, thereby increasing the efficiency of injection of hot electrons into the floating gate. This further translates into the operation of the cell at lower voltage. This is desirable. Therefore it is important for the floating gate to stick above the surface as far as possible in the Yoshida et al. design to increase the capacitance of C2 relative to the capacitance of C1.

The first problem with this strucuture is that it is impossible to fabricate by selective etchback of polysilicon to make the floating gate stick up above the top surface of the substrate by micron as the Yoshida et al. patent teaches. The intent of the Yoshida et al. structure, as illustrated in Figure 3-2 attached, is to increase the area of the C2 capacitor (represented by the area of the gate oxide layers 6-2) relative to the area of capacitor C1 (represented by the area of gate oxide layer 6-1).

Referring to Figures 3-2-1 through 3.2-4 and Figure 3A attached, the impossibility of building the Yoshida et al. structure is illustrated. One skilled in the art would attempt to build the Yoshida et al. structure by first etching a hole in silicon substrate, growing oxide layer 6 in Figure 3-2-1 in the hole, depositing polysilicon layer 7 over the gate oxide layer 6, and then doing an antisotropic etch of the polysilicon to remove the horizontal components as shown in Figure 3-2-2 attached. The problem is that when the anisotropic etch is done, the polysilicon layer 7 from which the floating gate 4 in Yoshida et al. will be fabricated, is even with the top of the thin gate oxide layer which is formed on top of the drain 9. The make the floating gate polysilicon 7 protrude above the surface of the substrate by one micron, one must attempt to selectively etch back the silicon of the drain area 9 without also etching away the polysilicon 7 of the floating gate so that the floating gate will stick up above the surface of the substrate and increase the area of one capacitor versus the other.

It is well known to those skilled in the art, that it is impossible to selectively etch the

substrate drain area 9 (which is silicon) away from the sides of the floating gate polysilicon 7 because both are silicon. Before any such selective etch of the drain area 9 in Figure 3-2-2 could be attempted, it would be required to remove the gate oxide layer 8 on top of the drain to expose the silicon of the drain to the etch process. Any oxide etch process would over etch the oxide and leave the divot shown at 10 in Figure 3-2-3. This divot would be of unknown depth and would depend upon the degree of overetching. Therefore, even if any selective etch of the drain 9 which did not also remove portions of the polysilicon 7 were possible, the amount of silicon drain material removed relative to the depth of the divot 10 would be unknown and this would create a potential short between the floating gate and the drain 9 or channel region 11. However, it is not possible to do a selective etch of the silicon of the drain 9without also etching the polysilicon 7 of the floating gate, so no protruding floating gate structure like that shown in Figure 3-2-4 could be built. Note that Figure 3-2-4 does not show the possible misalignment between the depth of the divot 10 of the gate oxide versus the amount of the drain area 9 which was removed. It would also be quite difficult or impossible to control the exact amount of drain material removed relative to floating gate polysilicon if such a selective etch were possible. This means it would be quite possible to etch entirely through the drain area 9 and leave no N+ doped drain area at all thereby rendering the transistor inoperative.

More specifically, to attempt to do this selective etch, one would have to first etch away portions of the floating gate polysilicon lying on oxide 8 on top of drain area 9 in Figure 3-2-1 after its deposit and stop at the very edge of the vertical cavity to form the structure shown in Figure 3-2-2. . This would leave the floating gate poly etched down to the top surface of the

substrate (which is covered by a layer of oxide[1]) as shown in Figure 3-2-2 and even with the top of the well. One would then have to selectively etch the silicon dioxide layer 8 on top of the drain 9 without etching the gate oxide 8' on the vertical wall of the well in Figure 3-2-2. This also is impossible, so the etch to remove the oxide 8 on top of the drain, would also etch away some unknown portion of the oxide 8' on the vertical wall of the well to leave a divot 10 of unknown depth as shown in Figure 3-2-3. . Then, one would have to somehow selectively etch the N+ doped silicon 9 of the drain area further down while leaving the floating gate polysilicon 7 extending above the top surface of the drain 9 to obtain a vertical wall of floating gate polysilicon sticking up above the top surface of the drain by one micron as required by the Yoshida et al. structure. This is not possible for the reasons explained above.

In other words, assume one formed the alternating P and N type layers 12, 11 and 9 (source, channel and drain, respectively) in the substrate, and then etched a vertical well, the wall of which is shown at 3 in Figures 3-2-1 through 3-2-4.. Then suppose one grew a layer of gate oxide 8 on the top surface of the substrate to insulate the top of the drain N+ region 9, and to insulate the the walls of the vertical well 3. Suppose one then deposited the first floating gate polysilicon 7 on top of the gate oxide 8 and 8' and down into the well 3. Suppose one then anisotropically etched the horizontal portions of the first polysilicon off the horizontal surfaces on the top of the substrate down to the gate oxide layer 8 and off the horizontal bottom of the well 3.. Then, to get vertical first polysilicon walls that stick up above the surface of the substrate, one would have to selectively etch the gate oxide 8 and the drain area 9 of the substrate down

---

to keep the floating gate poly from shorting to the drain area at the top of the substrate which surrounds the well.

about one micron without etching away the polysilicon 7 of the floating gate. This cannot be done, as there is no way to selectively etch monocrystalline silicon of the substrate drain area 9 without also etching the polysilicon 7 of the floating gate. One cannot make the gate oxide 1 micron thick, because that would make the gate oxide layer 8' insulating the floating gate 7 from the drain, source and channel regions too thick[2] and this would make capacitor C1 too small. Large thickness of gate oxide 8' will cause degradation of the floating gate's control over the threshold voltage of the transistor which is the whole point of injecting charge onto a floating gate to program a nonvolatile memory cell. Too thick of a layer of gate oxide 8' would probably also prevent any ability to alter the state of trapped charge in the floating gate by applying any realistic voltage to the control gate (5 in Figure 3 of the Yoshida et al. patent). Applying too large of a programming voltage (which would be required if the gate oxide layer 8' in Figure 3-2-1) would cause punch through somewhere on the device and destroy it by causing an unintended short or open somewhere where a short or open should not be.

Another approach one skilled in the art might attempt to build the Yoshida et al. structure would be as illustrated in Figures 3-3-1 through 3-3-4. In this approach, it would be necessary to form the three alternating P type and N type layers 9, 11 and 12 in the substate **and then grow a very thick field oxide layer 13 (as shown in Figure 3-3-1 attached) on the top surface (drain N+ layer 9) of the substrate to the thickness that you would like to have the floating gate polysilicon 7 stick above the top surface of the substrate *i.e.*, one micron.** Then one would etch the vertical wells (the vertical wall of this well is shown at 3 in Figure 3.3-

---

The Yoshida et al. patent teaches that the gate oxide is 150 angstroms thick in the preferred embodiment, at Col. 3, lines 21.

1), grow gate oxide 8' and deposit the first polysilicon 7 for the floating gate to arrive at the structure shown in Figure 3-3-1. Suppose one then anisotropically etched the first polysilicon layer 7 to remove all first polysilicon off horizontal surfaces to arrive at Figure 3-3-2. Then, suppose one selectively etched the field oxide 13 off the top surface of the substrate without removing the first polysilicon 7. This etch would remove the field oxide 13 down to the top of the silicon substrate drain region 9 but not remove the first polysilicon 7 so that it would stick up above the top of the substrate by about one micron. However, because the selective anisotropic etch cannot be precisely controlled, it would start to eat into the gate oxide layer 8' insulating the floating gate 7 from the drain layer 9 thereby leaving a divot 14 of unknown depth. This creates small divot or gap of the gate silicon dioxide (hereafter gate oxide) between the floating gate and the top of the drain layer of the substrate, as shown in Figure 3-3-3.

This little divot or gap between the floating gate and the drain represents a potential short between the floating gate and the drain, so it has to be repaired. To repair that divot,, more silicon dioxide would have to be grown on the top surface of the substrate to fill in the divot and prevent a short, and thick field oxide would also have to be grown on the top of the drain 9 The repair oxide and the thick field oxide are shown as layer 15 in Figure 3-3-4. However, it is required that the gate oxide between the control gate (shown at 16 in Figure 3-3-4) and the floating gate 7 be thin so that capacitor C2 can be large. When field oxide 15oxide is grown on top of the silicon substrate drain layer 9, oxide will also grow on top of the floating gate polysilicon 7 before the second polysilicon for the control gate 16 is deposited in the well. This will increase the thickness of the oxide between the floating gate 7 and the control gate 16 and decrease the value of the capacitor C2 which decreases the efficiency of hot electron injection into the floating gate. Increasing the capacitance of capacitor C2 relative to the capacitance of

C1 is the whole point of the Yoshida et al. design, so this side effect of repairing the divot and adding a sufficient thickness of field oxide is very undesirable.

If the oxide between the floating gate and the control gate is grown in the same step as the field oxide 15 over the drain region that insulates the control gate 16 from the drain 9 (which is logical), then the field oxide 15 grown on the top surface of the substrate to insulate the control gate 16 from the drain region 9 will be too thin since it must be grown to the same thickness as the gate oxide between the control gate 16 and the floating gate 7 to make C2 large (which is the whole point of the Yoshida et al. patent). This is because the oxide that is grown between the floating gate 7 and the control gate 16 must be thin so that capacitor C2 can be kept large. That, unfortunately, also means that the field oxide 15 formed on top of the substrate to insulate the control gate from the drain 9 will also be thin. This creates a danger of punch through between the control gate 16 and the drain 9 when programming voltage (typically 8-12 volts) is applied to the control gate 16. The reason is because the control gate is subjected to a high voltage to erase the device. Thus, unless the field oxide 15 between the control gate 16 and the drain 9 is thick enough (typically 1000-2000 angstroms), there will be a punch-through failure between the control gate 16 and the drain when the erase voltage is applied, and the device will be destroyed. 1000 to 2000 angstroms is too thick for the oxide between the control gate and the floating gate because it makes C2 too small and decreases the efficiency of hot electron injection into the floating gate.

The field oxide 15 between the control gate 16 and the drain 9 cannot be grown separately from the oxide layer 15' (see Figure 3-3-4 between the control gate 16 and the floating gate 7. This is because there is no self-aligned way to grow or etch oxide layer 15 so as to be thicker than interpoly oxide layer 15'. For example, if oxide layer 15 is grown thermally to

the required thickness of 1000-2000 angstrom, interpoly oxide layer 15' will also be 1000-2000 angstroms thick. This will completely oxidize through the 1000 angstrom thick portion of the floating gate 7 sticking up above the top surface of the substrate thereby destroying it. It may also completely oxidize through all of the floating gate portion down in the well. This process will completely remove the portion of the floating gate sticking up above the surface of the substrate and may destroy the floating gate altogether.

Even if this oxidation step did not completely oxidize the polysilicon of the floating gate in the well and sticking above the surface of the substrate, it would grow a layer of oxide 15' 1000-2000 angstroms on the vertical surfaces of the floating gate between the floating gate and the control gate. This is too thick of an oxide layer between the floating gate and the control gate, and would make the capacitance of capacitor C2 too small which is exactly the opposite of what the Yoshida et al. design is intended to do (capacitance is reduced as the thickness of the insulation between the plates of the capacitor is increased).

There is no way to grow this 1000-2000 angstrom thick oxide layer 15 over the drain 9 without making oxide layer 15' between the floating gate and the control gate just as thick. Further, there is no known etch process to remove only the vertical oxide from the walls of the floating gate 7 and leave the horizontal oxide components of layer 15 untouched. Because there is no selective or anisotropic etch to remove only the components of oxide on the vertical walls of the floating gate 7, this means a mask would have to be used to protect the vertical well from oxide growth so that oxide layer 15 can be grown to the required thickness of 1000-2000 angstroms without simultaneously increasing the thickness of interpoly oxide layer 15' insulating the control gate 16 from the floating gate 7. Such a mask would have to be exactly aligned with the edges of the vertical well 3, as shown in Figure 3-3-4 attached, and then a thick

field oxide layer 15 would have to be grown to arrive at the structure shown in Figure 3-3-6. If the mask was not exactly aligned, as shown in Figure 3-3-5 and Figure 3.3.7 (slight misalignment is always the case with any mask), it would cause a gap in the oxide under the overlap 17 or a field oxide layer 15" under the overlap 17 which was too thin (as explained further below). This would cause a short between the control gate 16 and the drain 9 when programming or erase voltages were applied.

To exactly align such a mask to cover only the mouth of the vertical well without any misalignment or overlap on any portion of the drain region 9 surrounding the well 3 would be impossible.

It cannot be emphasized enough, that the mask would have to be exactly aligned with the edges of the well 3 all the way around the perimeter of the well. The slightest mismatch between the perimeter of the well and the perimeter of the mask would mean that no oxide or too thin of a layer of field oxide would be grown on the drain region 9 where the misalignment overshadow occurred. The gap in the oxide (or too thin field oxide –hereafter referred to as a lack of oxide) covering the drain region would occur at all misalignments of the type where the mask overlapped the drain region slightly. This lack of oxide on the drain region where the overlap occurred would mean that the portion of the drain at the oxide gap would not be insulated (or would short to the control gate by a punch through) when the control gate second polysilicon is later deposited (or programming voltage is applied). Thus, when the control gate polysilicon 16 (shown in dashed lines in Figure 3-3-7) was deposited, it would go down into the oxide gap and make contact with the drain region 9 thereby causing a short between the the control gate and the drain (or causing a short later when programming or erase voltages were applied to the control gate 16). An actual short would usually result because the thin gate

oxided 15'' under the overlap 17 would be removed by the etch which removed the nitride mask 19. The exactly aligned case after removal of the nitride mask 19 and showing a narrow gap at 21 is shown in Figure 3-3-8. The misaligned case, which would always be the case, after the nitride mask 19 is removed and showing a big gap in oxide coverage at 21, is shown at Figure 3-3-9. Figure 3-3-10 and 3-3-11 show the shorts which would exist in the perfectly aligned and misaligned cases after control gate 16 is added.

To ensure that the well was protected from the oxidation step to grow field oxide layer 15, the mask 19 would have to be bigger than the well 3 to ensure the well was protected. But making the mask bigger than the size of the well would definitely cause a gap in the oxide insulating the control gate from the drain at all overlap points and render the device inoperative. There are no design rules which would allow use of a mask 19 that was exactly the size of the well and guaranteed exact alignment every time, and no self aligned way of forming this mask 19 in Figure 3-3-6 so as to be perfectly aligned exist.

Also, oxide grows much slower on single crystal silicon substrate than on the polysilicon of the floating gate. The difference in speed of growth ratio can be as much as 4:1. This means if a thin interpoly oxide layer 15' is grown, and the oxide over the substrate to insulate the drain from the control gate were grown in the same step, the result would be a very thin layer of field oxide 15 over the drain because of the much slower growth rate on the single crystal silicon of the drain region 9. This would result in a field oxide layer 15 over the drain which could be as much as 4 times thinner than the very thin interpoly gate oxide layer 15'. This would be too thin for an insulation layer protecting the drain 9 from the control gate 16 and would lead to a punch through failure at the location where the control gate overlaps this thin oxide over the drain when any high program or erase voltage is applied.

Therefore, it is my conclusion that the structure of Figures 3 and 5 in the Yoshida et al. patent cannot be built as shown and be operative.

Further, declarant sayeth not.

Dated:_____ _____

Ashok Kapoor